Intel® Q35/Q33/G33/P35 Express Chipset

Thermal and Mechanical Design Guidelines

— For the 82Q35, 82Q33, 82G33 Graphics and Memory Controller Hub (GMCH) and 82P35 Memory Controller Hub (MCH)

October 2007

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Revision History

Revision Number	Description	Date
-001	• Initial Release	June 2007
-002	• Added 82Q35 GMCH and 82Q33 GMCH information	August 2007
-003	• Updated Tcontrol value • Updated P35 $T_{C\text{-}MAX}$ specification	October 2007

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1 Introduction

As the complexity of computer systems increases, so do power dissipation requirements. The additional power of next generation systems must be properly dissipated. Heat can be dissipated using improved system cooling, selective use of ducting, and/or passive heatsinks.

The objective of thermal management is to ensure that the temperatures of all components in a system are maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors, or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component.

This document is for the following devices:

- Intel® Q35 Express Chipset GMCH (82Q35 GMCH)
- Intel® Q33 Express Chipset GMCH (82Q33 GMCH)
- Intel® G33 Express Chipset GMCH (82G33 GMCH)
- Intel® P35 Express Chipset MCH (82P35 MCH)

This document presents the conditions and requirements to properly design a cooling solution for systems that implement the (G)MCH. Properly designed solutions provide adequate cooling to maintain the (G)MCH case temperature at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the case to local-ambient thermal resistance. By maintaining the (G)MCH case temperature at or below those recommended in this document, a system designer can ensure the proper functionality, performance, and reliability of this component.

Note: Unless otherwise specified the information in this document applies to all configurations of Intel® 82Q35 GMCH, 82Q33 GMCH, 82G33 GMCH, and 82P35 MCH. The Intel® 82Q35 GMCH, 82Q33 GMCH, 82G33 GMCH contains integrated graphics and associated SDVO and analog display ports. In this document the integrated graphics version and is referred to as GMCH. The Intel® 82P35 does not contain integrated graphics and is referred to as MCH. The term (G)MCH is used when referring to all configurations.

Note: In this document the use of the term chipset refers to the combination of the (G)MCH and the Intel® ICH9. For ICH9 thermal details, refer to the *Intel® I/O Controller Hub 9 (ICH9) Thermal Design Guidelines.*

1.1 Terminology

Term	Description
FC-BGA	Flip Chip Ball Grid Array. A package type defined by a plastic substrate where a die is mounted using an underfill C4 (Controlled Collapse Chip Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. Note that the device arrives at the customer with solder balls attached.
Intel® ICH9	Intel® I/O Controller Hub 9. The chipset component that contains the primary PCI interface, LPC interface, USB, ATA, and/or other legacy functions.
GMCH	Graphic Memory Controller Hub. The chipset component that contains the processor and memory interface and integrated graphics core.
T_A	The local ambient air temperature at the component of interest. The ambient temperature should be measured just upstream of airflow for a passive heatsink or at the fan inlet for an active heatsink.
T_C	The case temperature of the (G)MCH component. The measurement is made at the geometric center of the die.
$T_{C\text{-}MAX}$	The maximum value of T_C.
$T_{C\text{-}MIN}$	The minimum valued of T_C.
TDP	Thermal Design Power is specified as the maximum sustainable power to be dissipated by the (G)MCH. This is based on extrapolations in both hardware and software technology. Thermal solutions should be designed to TDP.
TIM	Thermal Interface Material: thermally conductive material installed between two surfaces to improve heat transfer and reduce interface contact resistance.
Ψ_{CA}	Case-to-ambient thermal solution characterization parameter (Psi). A measure of thermal solution performance using total package power. Defined as (T_C – T_A) / Total Package Power. Heat source size should always be specified for Ψ measurements.

1.2 Reference Documents

Document	Location
Intel® Series 3 Express Chipset Family Datasheet	www.intel.com/design/chipsets/datashts/316966.htm
Intel® I/O Controller Hub 9 (ICH9) Family Thermal Design Guidelines	www.intel.com/design/chipsets/designex/316974.htm
Intel® Core™2 Extreme Quad-Core Processor and Intel® Core™2 Quad Processor Thermal and Mechanical Design Guidelines	http://developer.intel.com/design/processor/designex/315594.htm
Balanced Technology Extended (BTX) Interface Specification	http://www.formfactors.org
Various System Thermal Design Suggestions	http://www.formfactors.org
Various Chassis Thermal and Mechanical Design Suggestions	http://www.formfactors.org

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2 Product Specifications

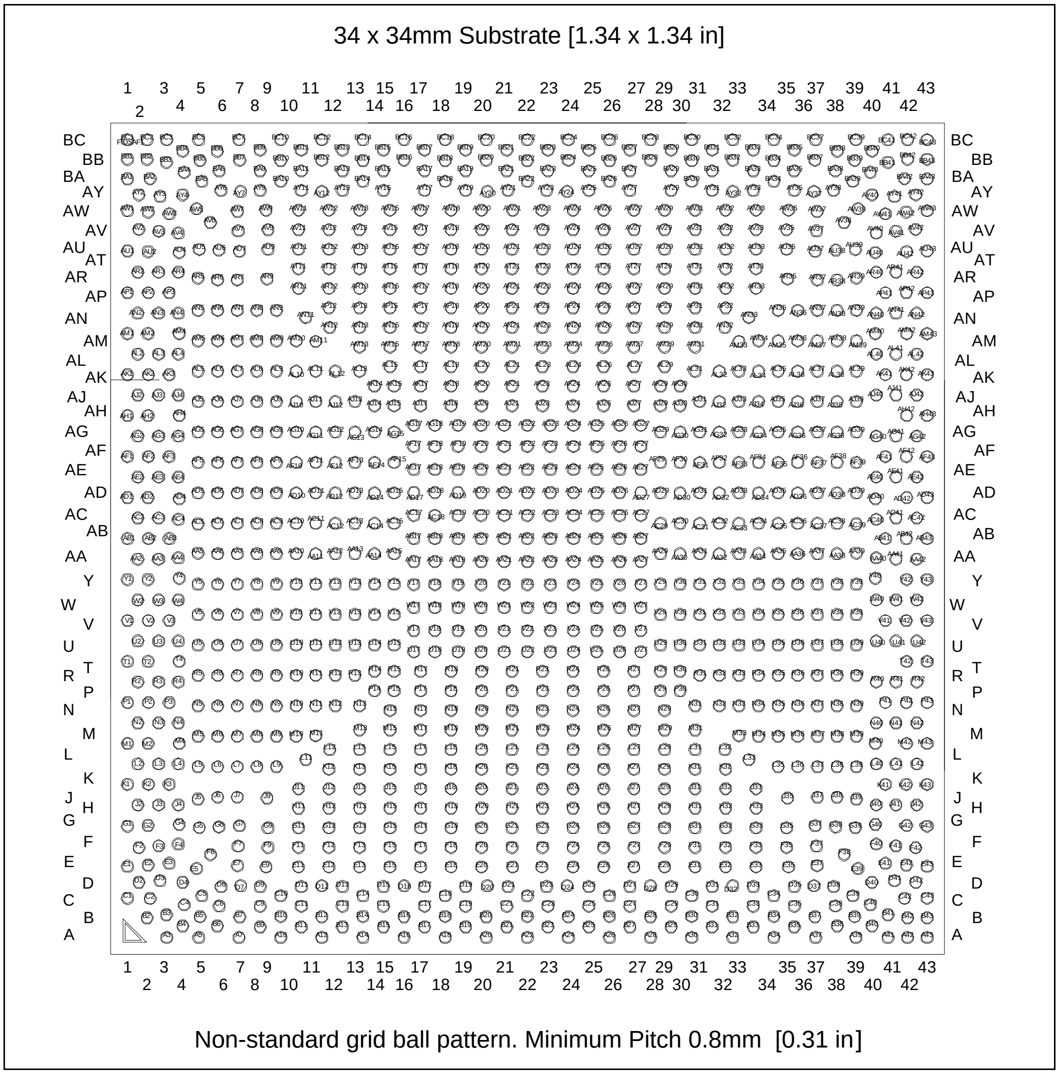
2.1 Package Description

The (G)MCH is available in a 34 mm [1.34 in] x 34 mm [1.34 in] Flip Chip Ball Grid Array (FC-BGA) package with 1226 solder balls. The die size is 10.41 mm [0.410 in] x 10.41 mm [0.410 in]. A mechanical drawing of the package is shown in Figure 13, Appendix B.

2.1.1 Non-Grid Array Package Ball Placement

The (G)MCH package uses a “balls anywhere” concept. Minimum ball pitch is 0.8 mm [0.031 in], but ball ordering does not follow a 0.8 mm grid. Board designers should ensure correct ball placement when designing for the non-grid array pattern. For exact ball locations relative to the package, refer to the *Intel® 3 Series Express Chipset Family Datasheet.*

Figure 1. (G)MCH Non-Grid Array



2.2 Package Loading Specifications

Table 1 provides static load specifications for the package. This mechanical maximum load limit should not be exceeded during heatsink assembly, shipping conditions, or standard use conditions. Also, any mechanical system or component testing should not exceed the maximum limit. The package substrate should not be used as a mechanical reference or load-bearing surface for the thermal and mechanical solution.

Table 1. Package Loading Specifications

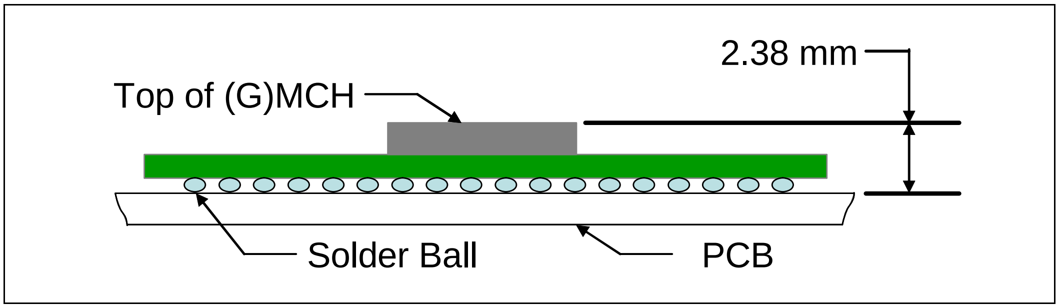
Parameter	Maximum	Notes
Static	15 lbf	1,2,3

NOTES:

1. These specifications apply to uniform compressive loading in a direction normal to the package.
2. This is the maximum force that can be applied by a heatsink retention clip. The clip must also provide the minimum specified load on the package.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only.

To ensure the package static load limit is not exceeded, the designer should understand the post reflow package height. Figure 2 shows the nominal post-reflow package height assumed for calculation of a heatsink clip preload of the reference design. Refer to the package drawing in Appendix B to perform a detailed analysis.

Figure 2. Package Height



2.3 Thermal Specifications

To ensure proper operation and reliability of the (G)MCH, the case temperature must be at or below the maximum value specified in Table 2. System and component level thermal enhancements are required to dissipate the heat generated and maintain the (G)MCH within specifications. Chapter 3 provides the thermal metrology guidelines for case temperature measurements.

2.3.1 Thermal Design Power (TDP)

2.3.1.1 Definition

Thermal design power (TDP) is the estimated power dissipation of the (G)MCH based on normal operating conditions including V_{CC} and $T_{C\text{-}MAX}$ while executing real worst-case power intensive applications. This value is based on expected worst-case data traffic patterns and usage of the chipset and does not represent a specific software application. TDP attempts to account for expected increases in power due to variation in (G)MCH current consumption due to silicon process variation, processor speed, DRAM capacitive bus loading and temperature. However, since these variations are subject to change, there is no assurance that all applications will not exceed the TDP value.

The system designer must design a thermal solution for the (G)MCH such that it maintains T_C below $T_{C\text{-}MAX}$ for a sustained power level equal to TDP. Note that the $T_{C\text{-}MAX}$ specification is a requirement for a sustained power level equal to TDP, and that the case temperature must be maintained at temperatures less than $T_{C\text{-}MAX}$ when operating at power levels less than TDP. This temperature compliance is to ensure component reliability. The TDP value can be used for thermal design if the thermal protection mechanisms are enabled. The (G)MCH incorporate a hardware-based fail-safe mechanism to keep the product temperature in spec in the event of unusually strenuous usage above the TDP power.

2.3.2 TDP Prediction Methodology

2.3.2.1 Pre-Silicon

In order to determine TDP for pre-silicon products in development, it is necessary to make estimates based on analytical models. These models rely on knowledge of the past (G)MCH power dissipation behavior along with knowledge of planned architectural and process changes that may affect TDP. Knowledge of applications available today and their ability to stress various aspects of the (G)MCH is also included in the model. The projection for TDP assumes (G)MCH operation at $T_{C\text{-}MAX}$. The TDP estimate also accounts for normal manufacturing process variation.

2.3.2.2 Post-Silicon

Once the product silicon is available, post-silicon validation is performed to assess the validity of pre-silicon projections. Testing is performed on both commercially available and synthetic high power applications and power data is compared to pre-silicon estimates. Post-silicon validation may result in a small adjustment to pre-silicon TDP estimates.

2.3.3 Thermal Specifications

The data in Table 2 is based on post-silicon power measurements for the (G)MCH. The TDP values are based on system configuration with two (2) DIMMs per channel, DDR2 (or DDR3) and the FSB operating at the top speed allowed by the chipset with a processor operating at that system bus speed. Intel recommends designing the (G)MCH thermal solution to the highest system bus speed and memory frequency for maximum flexibility and reuse. The (G)MCH packages have poor heat transfer capability into the board and have minimal thermal capability without thermal solutions. Intel requires that system designers plan for an attached heatsink when using the (G)MCH.

Table 2. Thermal Specifications

Component	Memory Type	System Bus Speed	Memory Frequency	Idle	TDP	$T_{C\text{-}MIN}$	$T_{C\text{-}MAX}$	Notes
82G33 GMCH	DDR3	1333 MT/s	1066 MT/s	5.75 W	14.5 W	0 °C	106°C	1,2,3,4
82Q33 GMCH	DDR2	1333 MT/s	800 MT/s	5.5 W	13 W	0 °C	106 °C	1,2,3,5
82Q35 GMCH	DDR2	1333 MT/s	800 MT/s	5.5 W	13 W	0 °C	106 °C	1,2,3,5
82P35 MCH	DDR3	1333 MT/s	1066 MT/s	5.9 W	16.0 W	0 °C	106 °C	1,2,3,4

NOTES:
1. Thermal specifications assume an attached heatsink is present.
2. Max Idle power is the worst case idle power in the system booted to Windows* with no background applications running.
3. TDP is measured with DDR2 (or DDR3) with 2 channels, 2 DIMMs per channel and Max Idle power is measured with DDR2 (or DDR3) with 2 channels, 1 DIMM per channel.
4. Max Idle data is measured on 82G33, 82Q33 and 82Q35 GMCH for Energy Star with C2 / ASPM enabled.
5. Max Idle data is measured on 82P35 MCH for Energy Star when an external graphics card is installed in a system wherein this card must support L0s /L1 ASPM.
6. When an external graphics card is installed in a system with the Intel 82G33, 82Q33 or 82Q35, the TDP for these parts will assume the worst possible PCI Express design and consume as much as 82P35 TDG (16.0 W)

2.3.4 $T_{CONTROL}$ Limit

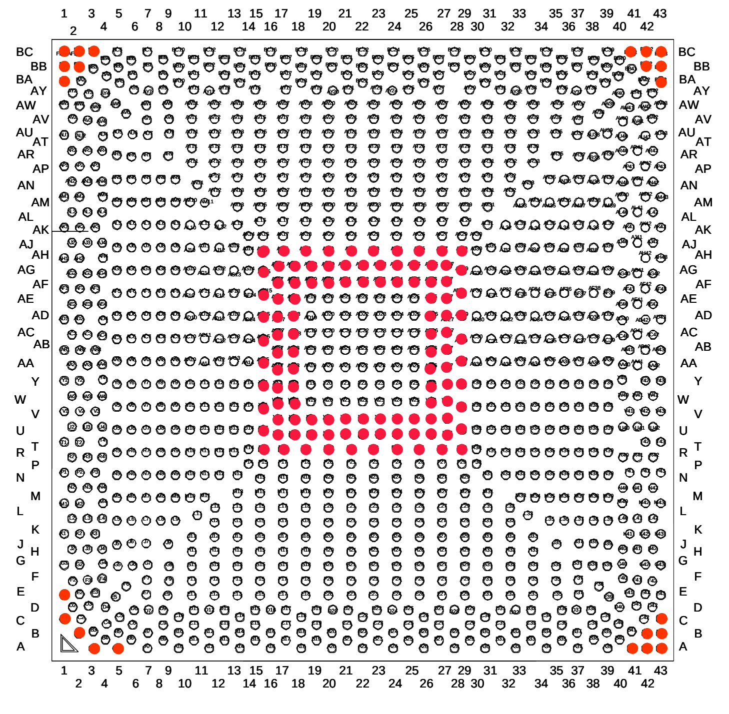
Intel® Quiet System Technology (Intel® QST) can monitor an embedded thermal sensor. The maximum operating limit when monitoring this thermal sensor is $T_{CONTROL}$. For the (G)MCH, this value is 97 °C. This value should be programmed into the appropriate register of Intel® QST, as the maximum sensor temperature for operation of the (G)MCH.

Note: For a complete discussion of programming the Intel® QST, consult the *Intel® Quiet System Technology (Intel® QST) Configuration and Tuning Manual*.

2.4 Non-Critical to Function Solder Balls

Intel has defined selected solder joints of the (G)MCH as non-critical to function (NCTF) when evaluating package solder joints post environmental testing. The (G)MCH signals at NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality. Figure 3 identifies the NCTF solder joints of the (G)MCH package.

Figure 3. Non-Critical to Function Solder Balls



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3 Thermal Metrology

The system designer must measure temperatures in order to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques of measuring (G)MCH component case temperatures.

3.1 Case Temperature Measurements

To ensure functionality and reliability of the (G)MCH the T_C must be maintained at or below the maximum temperature listed in Table 2. The surface temperature measured at the geometric center of the die corresponds to T_C. Measuring T_C requires special care to ensure an accurate temperature reading.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce error in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple bead and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, or contact between the thermocouple cement and the heatsink base (if a heatsink is used). To minimize these measurement errors a thermocouple attach with a zero-degree methodology is recommended.

3.1.1 Thermocouple Attach Methodology

1. Mill a 3.3 mm [0.13 in] diameter hole centered on bottom of the heatsink base. The milled hole should be approximately 1.5 mm [0.06 in] deep.
2. Mill a 1.3 mm [0.05 in] wide slot, 0.5 mm [0.02 in] deep, from the centered hole to one edge of the heatsink. The slot should be in the direction parallel to the heatsink fins (see Figure 5).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller K-type thermocouple bead to the center of the top surface of the die using a cement with high thermal conductivity. During this step, make sure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see Figure 4).
6. Attach heatsink assembly to the (G)MCH, and route thermocouple wires out through the milled slot.

Figure 4. 0° Angle Attach Methodology (top view, not to scale)

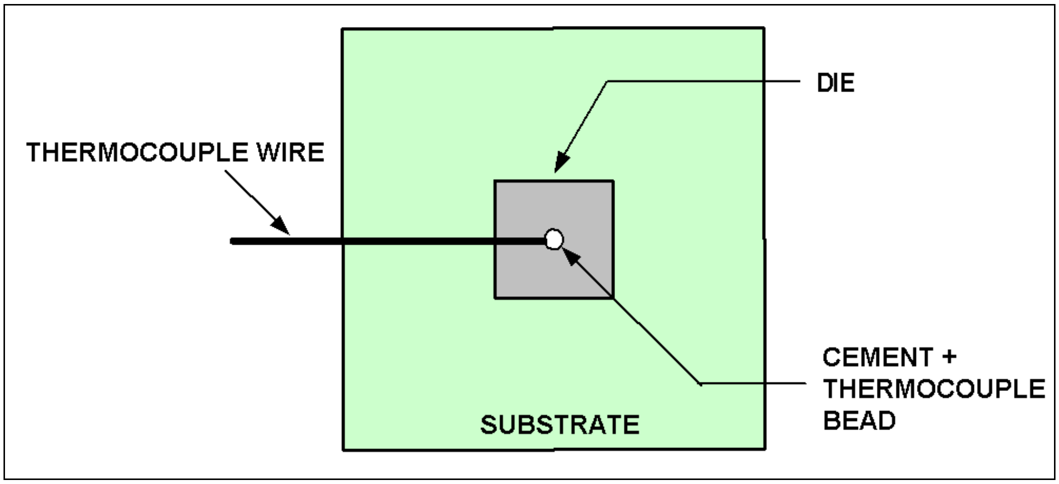
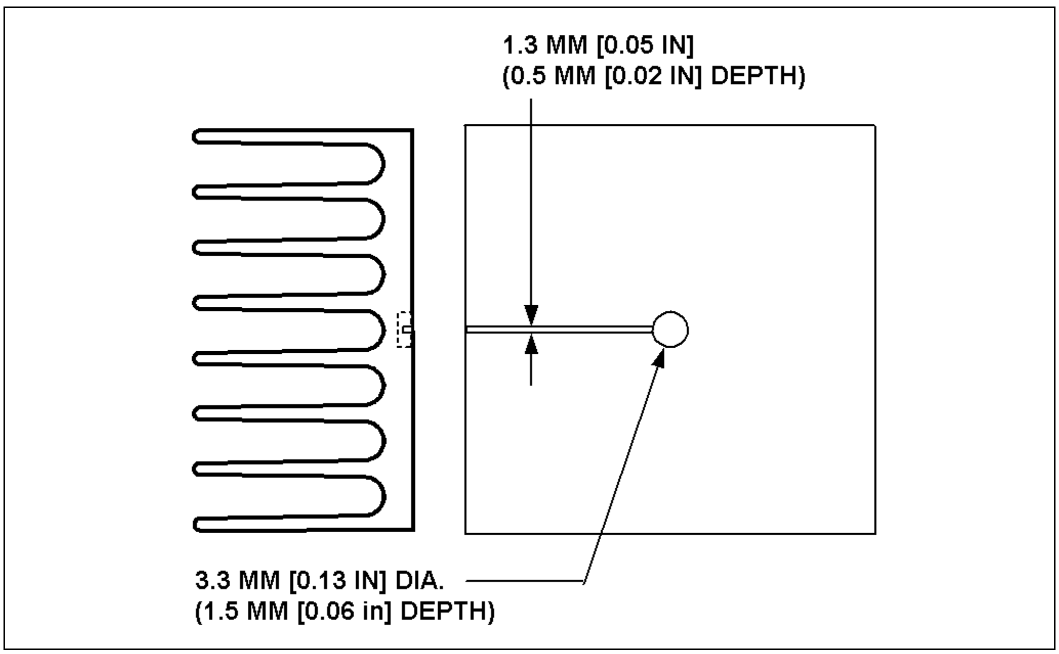


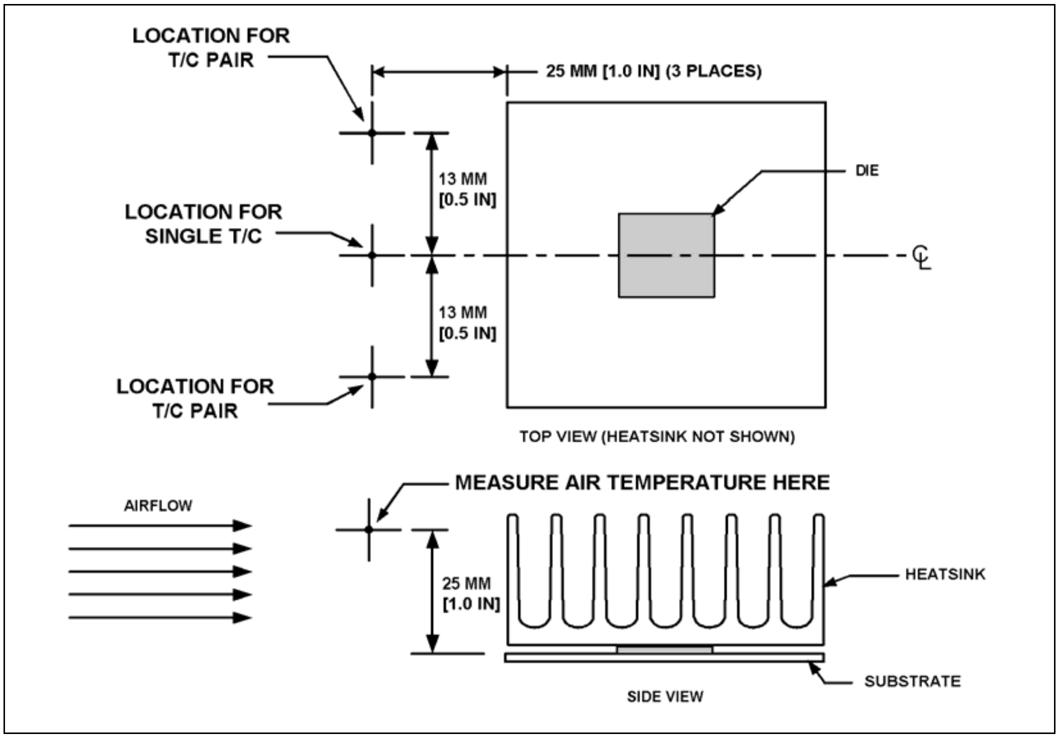
Figure 5. 0° Angle Attach Heatsink Modifications (generic heatsink side and bottom view shown, not to scale)



3.2 Airflow Characterization

Figure 6 describes the recommended location for air temperature measurements measured relative to the component. For a more accurate measurement of the average approach air temperature, Intel recommends averaging temperatures recorded from two thermocouples spaced about 25 mm [1.0 in] apart. Locations for both a single thermocouple and a pair of thermocouples are presented.

Figure 6. Airflow &Temperature Measurement Locations



Airflow velocity can be measured using sensors that combine air velocity and temperature measurements. Typical airflow sensor technology may include hot wire anemometers. Figure 6 provides guidance for airflow velocity measurement locations which should be the same as used for temperature measurement. These locations are for a typical JEDEC test setup and may not be compatible with chassis layouts due to the proximity of the processor to the (G)MCH. The user may have to adjust the locations for a specific chassis. Be aware that sensors may need to be aligned perpendicular to the airflow velocity vector or an inaccurate measurement may result. Measurements should be taken with the chassis fully sealed in its operational configuration to achieve a representative airflow profile within the chassis.

3.3 Thermal Mechanical Test Vehicle

A Thermal Mechanical Test Vehicle (TMTV) that provided by Intel is available for early thermal testing prior to the availability of actual silicon. The TMTV contains a heater die and can be powered up to a desired power level to simulate the heating of a (G)MCH package. The TMTV also contains daisy chain functionality and can be used for mechanical testing. The TMTV needs to be surface mounted to a custom board designed to provide connectivity to the die heater and/or daisy chain depending on the needs of the user. The package ball connections are provided so the user may design and build a board to interface with the TMTV. Note that although the TMTV is designed to closely match the (G)MCH package mechanical form and fit, it is recommended that final validation be performed with actual production silicon. The TMTV mechanical features, including die size, ball count, etc., may not reflect those of the final production package.

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4 Reference Thermal Solution

The design strategy for the reference thermal solution for the (G)MCH for use in ATX platforms reuses the ramp retainer and MB anchors from the Intel® G965 Express Chipset thermal solution. The extrusion design and a wire preload clip requirements are being evaluated for changes necessary to meet the (G)MCH thermal requirements. The thermal interface material and keep out zone remains the same as used with the Intel G965 Express Chipset (see Figure 14).

The BTX reference design for the (G)MCH will be similar to the Intel® G965 Express Chipset thermal solution. The thermal interface material, extrusion design and a wire preload clip requirements are being evaluated for changes necessary to meet the (G)MCH thermal requirements. The keep out zone remains the same as used with the Intel® G965 Express Chipset (see Figure 15).

This chapter provides detailed information on operating environment assumptions, heatsink manufacturing, and mechanical reliability requirements for the (G)MCH.

4.1 Operating Environment

The operating environment of the (G)MCH will differ depending on system configuration and motherboard layout. This section defines operating environment boundary conditions that are typical for ATX and BTX form factors. The system designer should perform analysis in the expected platform operating environment to assess impact on thermal solution selection.

4.1.1 ATX Form Factor Operating Environment

In ATX platforms, an airflow speed of 1.21 m/s [240lfm] is assumed to be approaching the heatsink at a 30° angle from the processor thermal solution (see Figure 7 and Figure 8 for more details). The local ambient air temperature, $T_{A,}$, at the (G)MCH heatsink in an ATX platform is assumed to be 45.6 °C for the (G)MCH. The airflow assumed above can be achieved by using a processor heatsink providing omni-directional airflow (such as a radial fin or “X” pattern heatsink). Such a heatsink can deliver airflow to both the (G)MCH and other areas like the voltage regulator, as shown in Figure 9. In addition, (G)MCH board placement should ensure that the (G)MCH heatsink is within the air exhaust area of the processor heatsink.

Note that heatsink orientation alone does not ensure that airflow speed will be achieved. The system integrator should use analytical or experimental means to determine whether a system design provides adequate airflow speed for a particular (G)MCH heatsink.

The thermal designer must carefully select the location to measure airflow to get a representative sampling. ATX platforms need to be designed for the worst-case thermal environment, typically assumed to be 35°C ambient temperature external to the system measured at sea level.

Figure 7. ATX Boundary Conditions

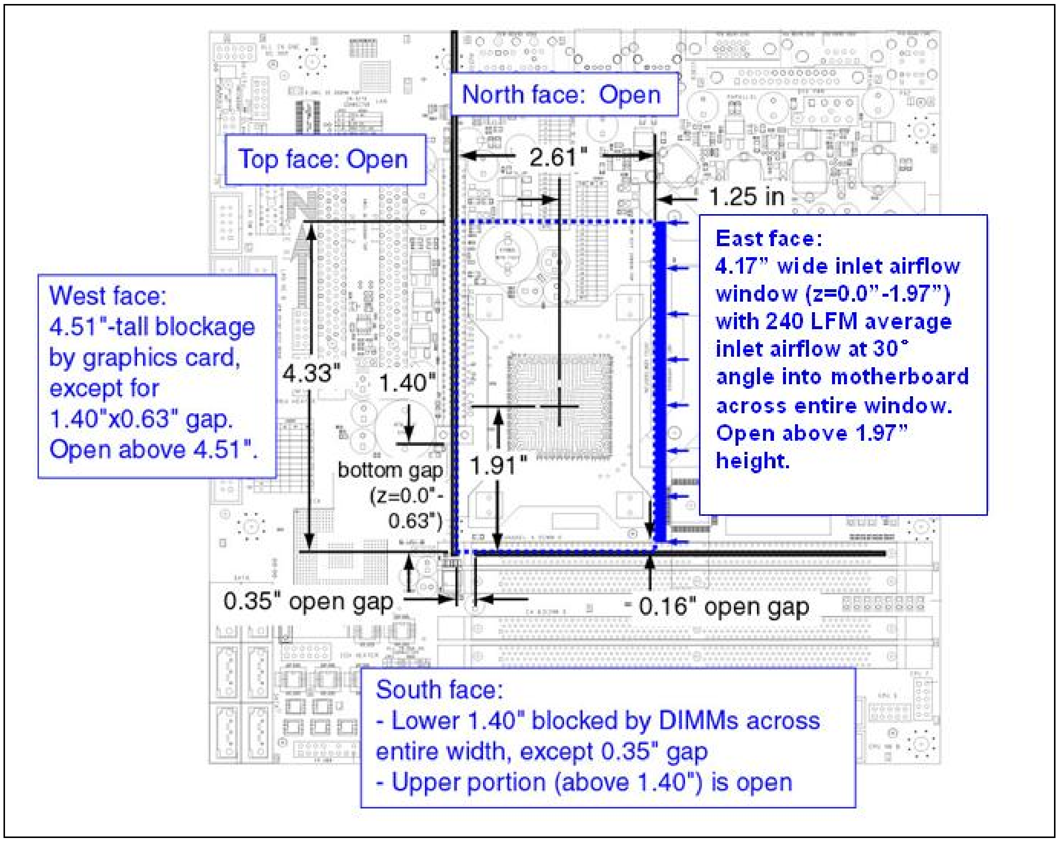


Figure 8. Side View of ATX Boundary Conditions

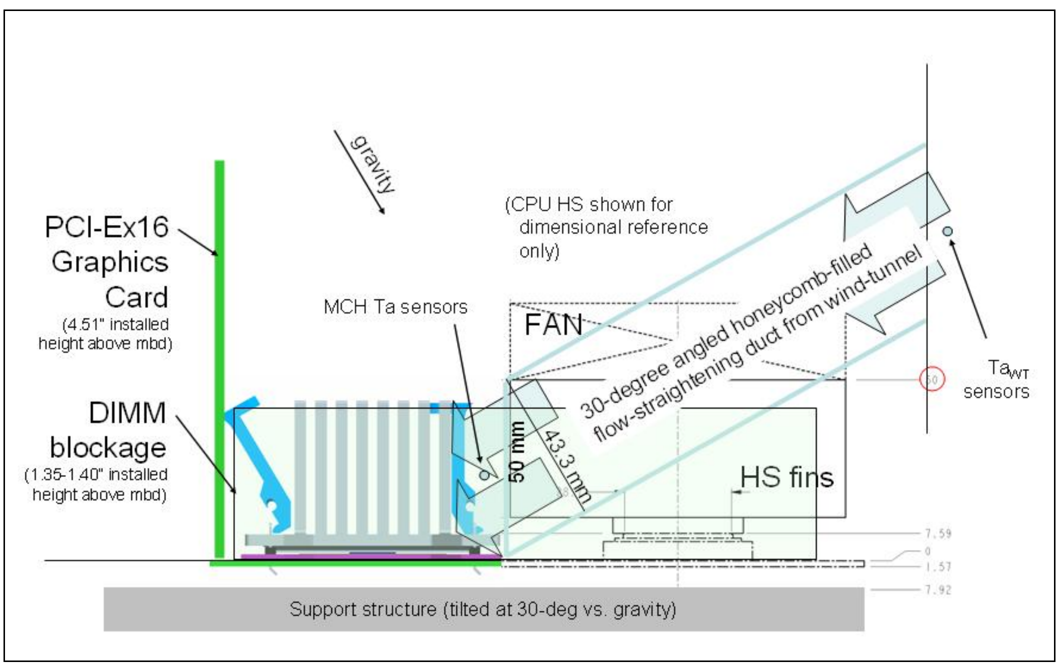
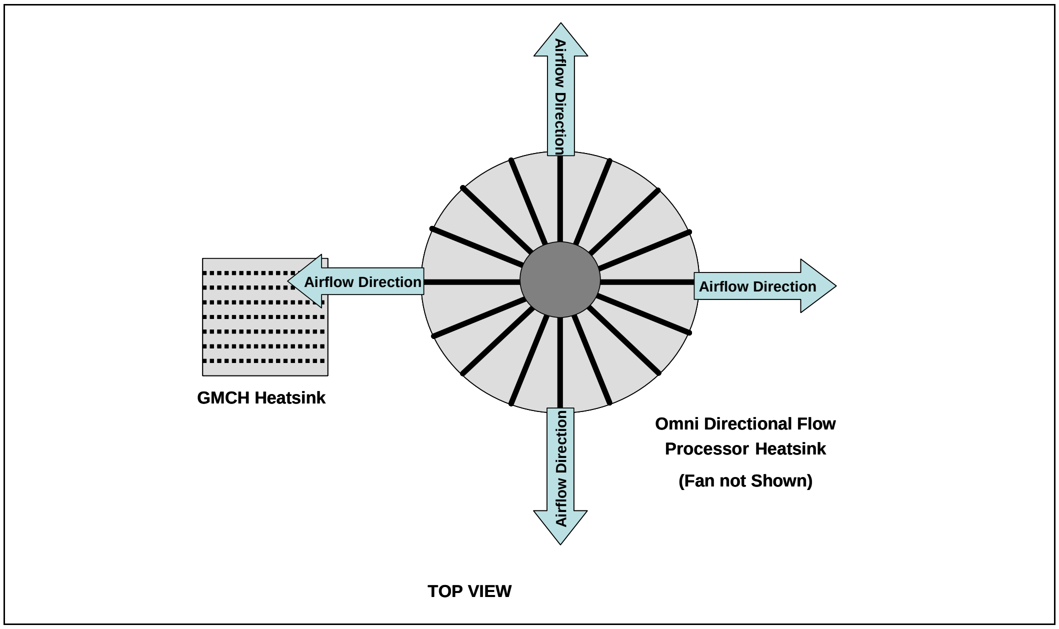


Figure 9. Processor Heatsink Orientation to Provide Airflow to (G)MCH Heatsink on an ATX Platform



Other methods exist for providing airflow to the (G)MCH heatsink, including the use of system fans and/or ducting, or the use of an attached fan (active heatsink).

4.1.2 Balanced Technology Extended (BTX) Form Factor Operating Environment

This section provides operating environment conditions based on what has been exhibited on the Intel micro-BTX reference design. On a BTX platform, the (G)MCH obtains in-line airflow directly from the processor thermal module. Since the processor thermal module provides lower inlet temperature airflow to the processor, reduced inlet ambient temperatures are also often seen at the (G)MCH as compared to ATX. An example of how airflow is delivered to the (G)MCH on a BTX platform is shown in Figure 10.

A set of three system level boundary conditions will be established to determine (G)MCH thermal solution requirement.

- Low external ambient (23 °C)/ idle power for the components (Case 3). This covers the system idle acoustic condition
- Low external ambient (23 °C)/ TDP for the components (Case 2). The TMA fan speed is limited by the thermistor in the fan hub.
- High ambient (35 °C)/ TDP for the components (Case 1). This covers the maximum TMA fan speed condition.

In addition to the 3 cases listed above the analysis considered both microtower and 3”-thick ePC chassis configurations to determine the worst case: The values in Table 3 correspond to the ePC configuration. For more details on the TMA airflow set points, refer to the *Balanced Technology Extended (BTX) System Design Guide.*

Table 3. Projected Chassis Conditions by Case

	T_A into MCH heatsink (°C)	Airflow into the (G)MCH heatsink (LFM)
Case 1	45.2	139
Case 2	42.0	68.8
Case 3	34.7	32.4

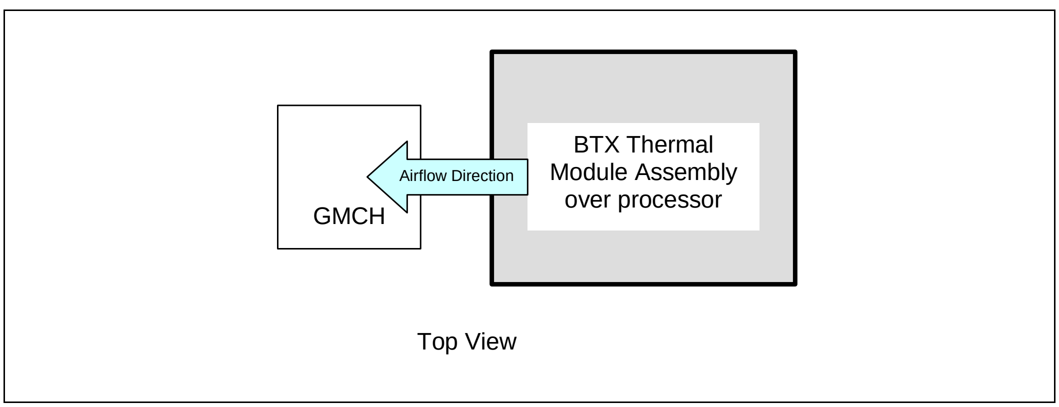
NOTES:
1. For all cases a thermal solution is required on the (G)MCH
2. These values are supplied based on final design review.

The customer should analyze their system design to verify their applicable boundary conditions prior to design. The thermal designer must carefully select the location to measure airflow to get a representative sampling. BTX platforms need to be designed for the worst-case thermal environment, typically assumed to be 35°C ambient temperature external to the system measured at sea level.

Note: The local ambient air temperature is a projection based on the power on a 2007 platform, processor TDP up to 65 W, and is subject to change in the next revision of this document.

Note: The risk of the solder ball fracture can be minimized with good chassis structure design on a BTX platform, refer to the *Balanced Technology Extended (BTX) Chassis Design Guide (or Balanced Technology Extended (BTX) System Design Guide) for detail chassis mechanical design.*

Figure 10. Processor Heatsink Orientation to Provide Airflow to (G)MCH Heatsink on a Balanced Technology Extended (BTX) Platform



4.2 Reference Design Mechanical Envelope

The motherboard component keep-out restrictions for the (G)MCH on an ATX platform are included in Appendix B, Figure 14. The motherboard component keep-out restrictions for the (G)MCH on a BTX platform are included in Appendix B, Figure 15.

4.3 Thermal Solution Assembly

The reference thermal solution for the (G)MCH for an ATX chassis is shown in Figure 11 and is an aluminum extruded heatsink that uses two ramp retainers, a wire preload clip, and four motherboard anchors. Refer to Appendix B for the mechanical drawings. The heatsink is attached to the motherboard by assembling the anchors into the board, placing the heatsink, with the wire preload clip over the (G)MCH and anchors at each of the corners, and securing the plastic ramp retainers through the anchor loops before snapping each retainer into the fin gap. Leave the wire preload clip loose in the extrusion during the wave solder process. The assembly is then sent through the wave process. Post wave, the wire preload clip is snapped into place on the hooks located on each of the ramp retainers. The clip provides the mechanical preload to the package. This mechanical preload is necessary to provide both sufficient pressure to minimize thermal contact resistance and to improve solder ball joint reliability. The mechanical stiffness and orientation of the extruded heatsink also provides protection to reduce solder ball reliability risk. A thermal interface material (*Honeywell PCM45F*) is pre-applied to the heatsink bottom over an area which contacts the package die.

The design concept for the (G)MCH in a BTX chassis is shown in Figure 12. The heatsink is extruded aluminum and uses a Z-clip for attachment. The clip is secured to the system motherboard via two solder down anchors around the (G)MCH. The clip helps to provide a mechanical preload to the package via the heatsink. This mechanical preload is necessary to provide both sufficient pressure to minimize thermal contact resistance and improvement for solder ball joint reliability. The mechanical stiffness and orientation of the extruded heat sink also provides protection to reduce solder ball reliability risk. A thermal interface material (*Honeywell PCM45F*) will be pre-applied to the heatsink bottom over an area in contact with the package die.

Note: To minimize solder ball joint reliability risk, the BTX Z-clip heatsink is intended to be used with the Support Retention Mechanism (SRM) described in the *Balanced Technology Extended (BTX) Interface Specification.* For additional information on designing the BTX chassis to minimize solder ball joint reliability, refer to the *Balanced Technology Extended (BTX) Chassis Design Guide.*

Figure 11. Design Concept for ATX (G)MCH Heatsink - Installed on Board

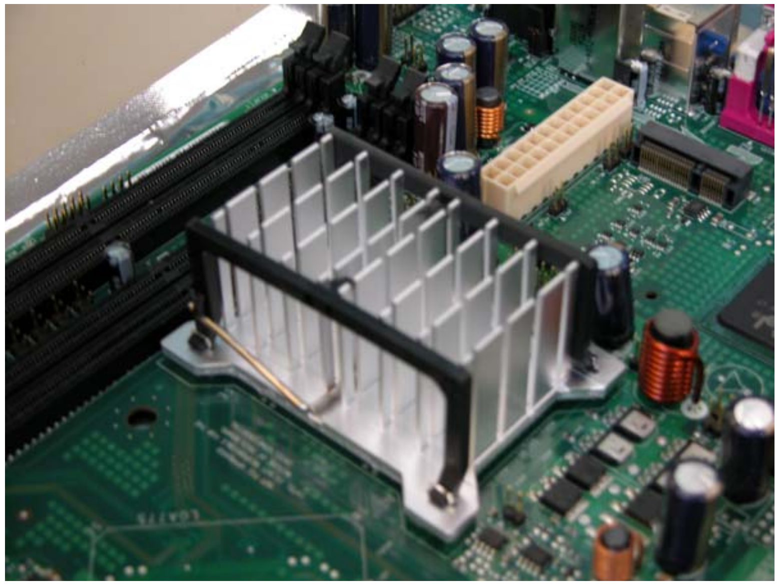
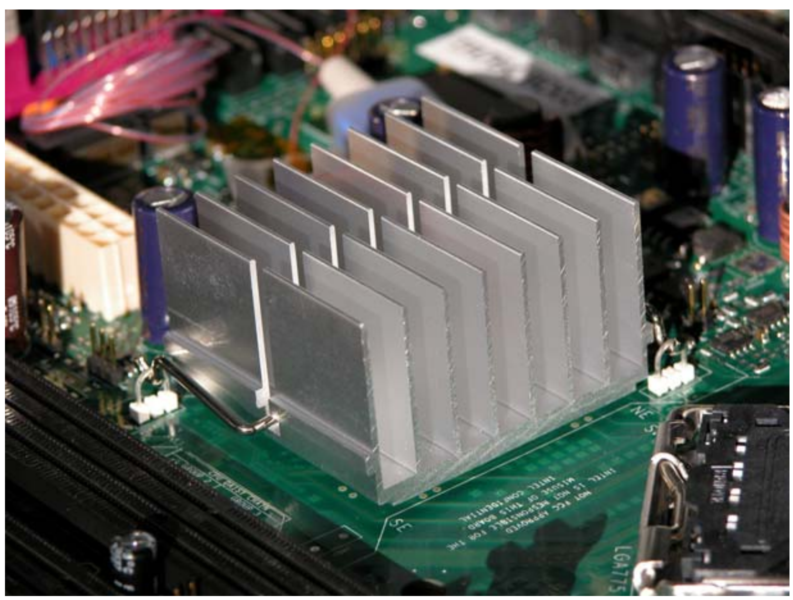


Figure 12. Design Concept for Balanced Technology Extended (BTX) (G)MCH Heatsink Design - Installed on Board



4.4 Environmental Reliability Requirements

The environmental reliability requirements for the reference thermal solution are shown in Table 4 and Table 5. These should be considered as general guidelines. Validation test plans should be defined by the user based on anticipated use conditions and resulting reliability requirements.

The ATX testing will be performed with the sample board mounted on a test fixture and includes a processor heatsink with a mass of 550g. The test profiles are unpackaged board level limits.

Table 4. ATX Reference Thermal Solution Environmental Reliability Requirements (Board Level)

Test[1]	Requirement	Pass/Fail Criteria[2]
Mechanical Shock	• 3 drops for + and - directions in each of 3 perpendicular axes (i.e., total 18 drops). • Profile: 50 G, Trapezoidal waveform, 4.3 m/s [170 in/s] minimum velocity change	Visual\Electrical Check
Random Vibration	• Duration: 10 min/axis, 3 axes • Frequency Range: 5 Hz to 500 Hz • Power Spectral Density (PSD) Profile: 3.13 g RMS	Visual/Electrical Check
Thermal Cycling	• -40 °C to +85 °C, TBD cycles	Thermal Performance
Unbiased Humidity	• 85 % relative humidity / 55 °C, TBD hours	Visual Check

NOTES:

1. The above tests should be performed on a sample size of at least 12 assemblies from 3 different lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.

The current plan for BTX reference solution testing is to mount the sample board mounted in a representative BTX chassis with a thermal module assembly having a mass of 900g. The test profiles are unpackaged system level limits.

Table 5. Balanced Technology Extended (BTX) Reference Thermal Solution Environmental Reliability Requirements (System Level)

Test[1]	Requirement	Pass/Fail Criteria[2]
Mechanical Shock	• 2 drops for + and - directions in each of 3 perpendicular axes (i.e., total 12 drops). • Profile: 25g, Trapezoidal waveform, 5.7 m/s [225 in/sec] minimum velocity change.	Visual\Electrical Check
Random Vibration	• Duration: 10 min/axis, 3 axes • Frequency Range: .001 g2/Hz @ 5Hz, ramping to .01 g2/Hz @20 Hz, .01 g2/Hz @ 20 Hz to 500 Hz • Power Spectral Density (PSD) Profile: 2.20 g RMS	Visual/Electrical Check
Thermal Cycling	• -40 °C to +85 °C, TBD cycles	Thermal Performance
Unbiased Humidity	• 85 % relative humidity / 55 °C, 500 hours	Visual Check

NOTES:

1. The above tests should be performed on a sample size of at least 12 assemblies from 3 different lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.
3. Mechanical Shock minimum velocity change is based on a system weight of 20 lbs to 29 lbs.
4. For the chassis level testing the system will include: 1 HD, 1 ODD, 1 PSU, 2 DIMMs and the I/O shield.

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Appendix A Enabled Suppliers

Enabled suppliers for the (G)MCH reference thermal solution are listed in Table 6 and Table 7. The supplier contact information is listed in Table 8.

Note: These vendors and devices are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

Table 6. ATX Intel® Reference Heatsink Enabled Suppliers for Intel 3 Series Chipsets

ATX Items	Intel PN	AVC	CCI	Foxconn	Wieson
Heatsink & TIM	D77030-001	S907C00002			
Plastic Clip	C85370-001	P109000024	334C863501A	3EE77-002	
Wire Clip	D29082-001	A208000233	334I833301A	3KS02-155	
Anchor	C85376-001			2Z802-015	G2100C888-143

Table 7. BTX Intel® Reference Heatsink Enabled Suppliers for Intel 3 Series Chipsets

BTX Items	Intel PN	AVC	Foxconn	Wieson
Heatsink assembly (HS/TIM & Wire Clip)	D75473-001	S906Z00001		
Anchor (Lead Free)	A13494-008		HB9703E-DW	G2100C888-064H

Table 8. Supplier Contact Information

Supplier	Contacts	Phone	Email
AVC (Asia Vital Components)	David Chao	+886-2-2299-6930 ext. 7619	david_chao@avc.com.tw
	Raichel Hsu	+886-2-2299-6930 ext. 7630	raichel_hsi@avc.com.tw
CCI(Chaun Choung Technology)	Monica Chih	+886-2-2995-2666	monica_chih@ccic.com.tw
	Harry Lin	(714) 739-5797	hlinack@aol.com
Foxconn	Jack Chen	(408) 919-6121	jack.chen@foxconn.com
	Wanchi Chen	(408) 919-6135	wanchi.chen@foxconn.com
Wieson Technologies	Beatrice Chang	+886-2-2647-1896 ext. 6395	beatrice@wieson.com
	Edwina Chu	+886-2-2647-1896 ext. 6390	edwina@wieson.com

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Appendix B Mechanical Drawings

The following table lists the mechanical drawings available in this document.

Figure 13. Intel® 3 Series Chipsets Package Drawing

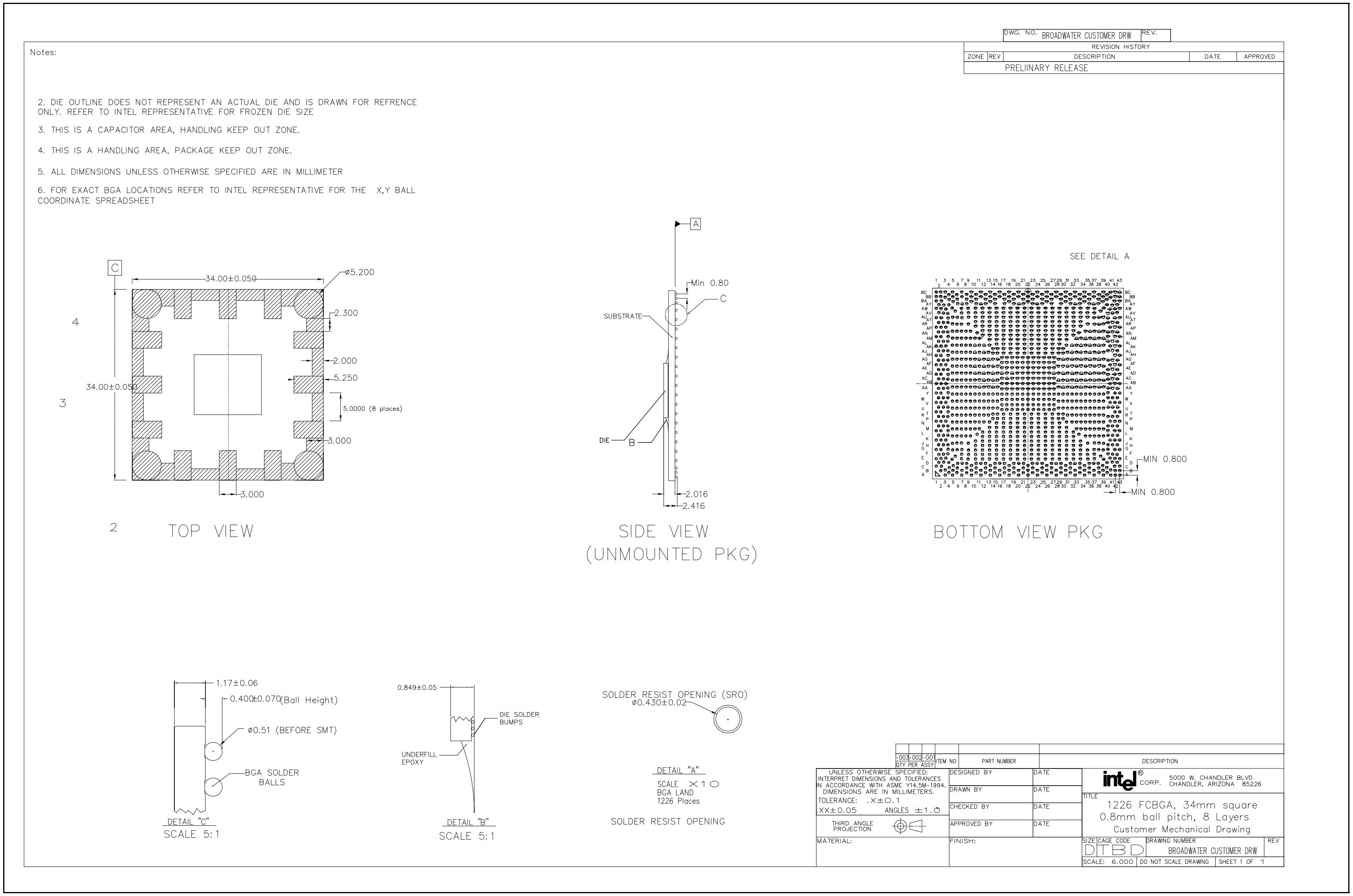


Figure 14. Intel® 3 Series Chipsets Component Keep-Out Restrictions for ATX Platforms

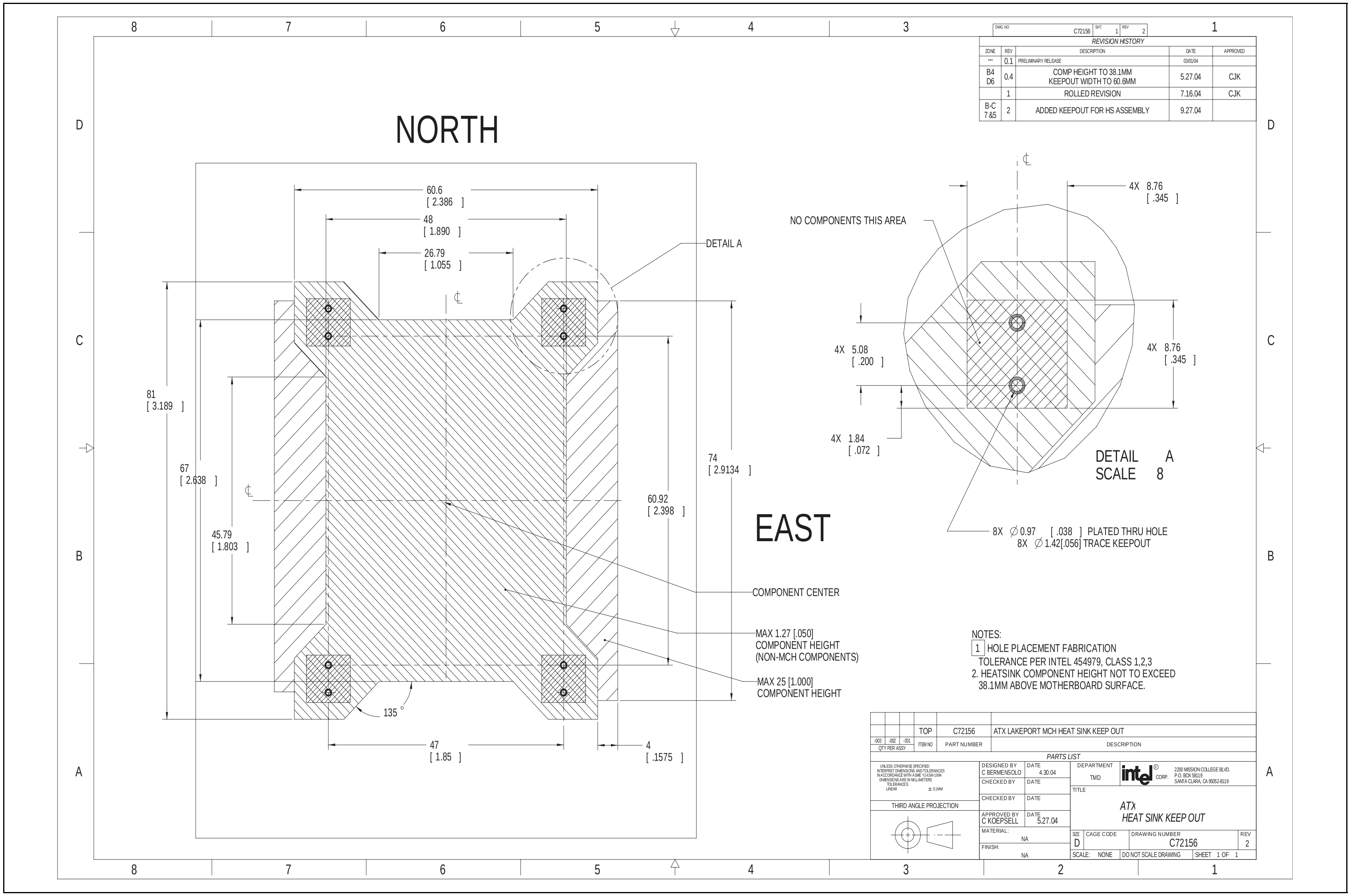


Figure 15. Intel® 3 Series Chipsets Component Keep-Out Restrictions for Balanced Technology Extended (BTX) Platforms

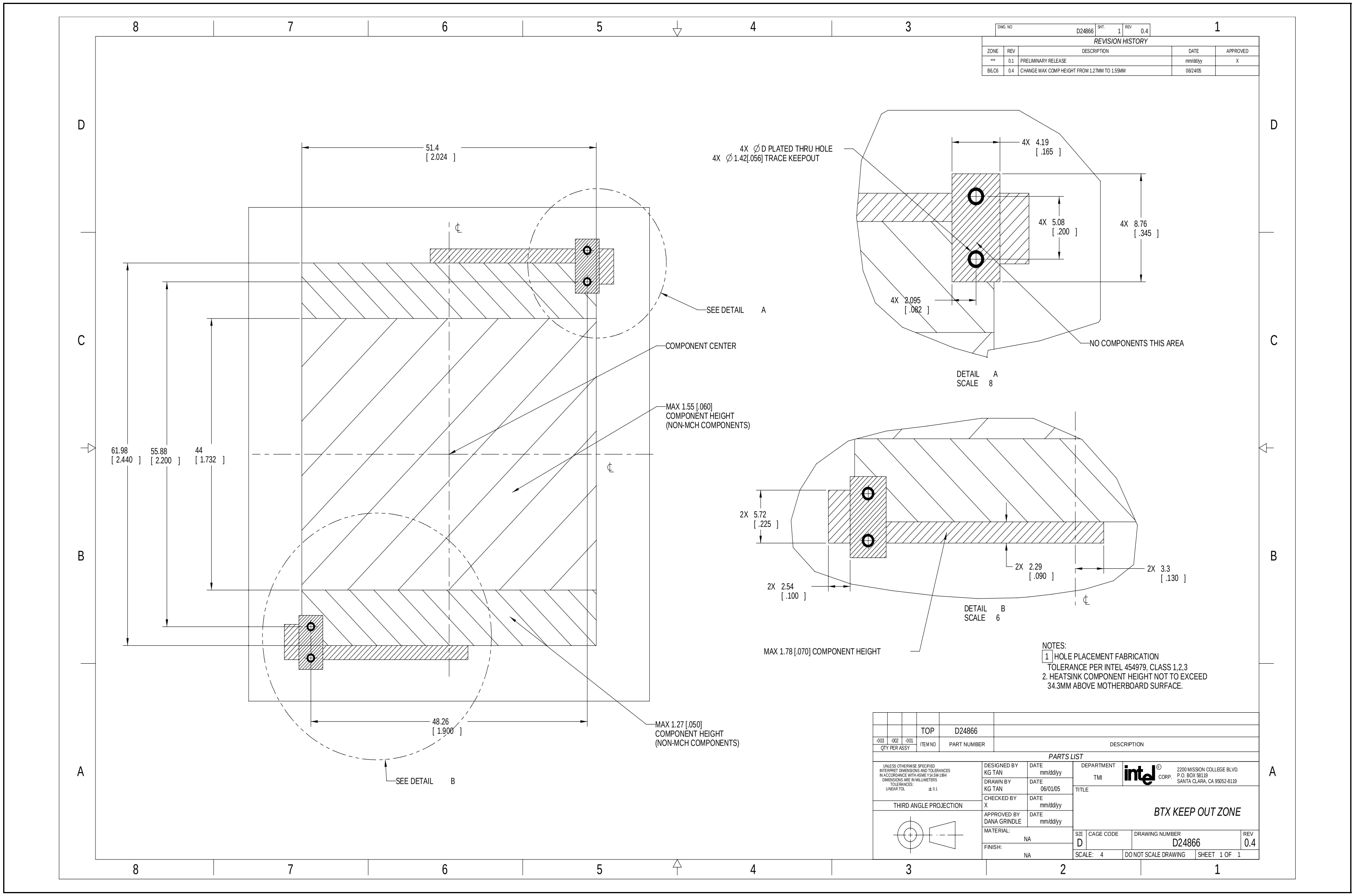


Figure 16. Intel® 3 Series Chipsets Reference Heatsink for ATX Platforms – Sheet 1

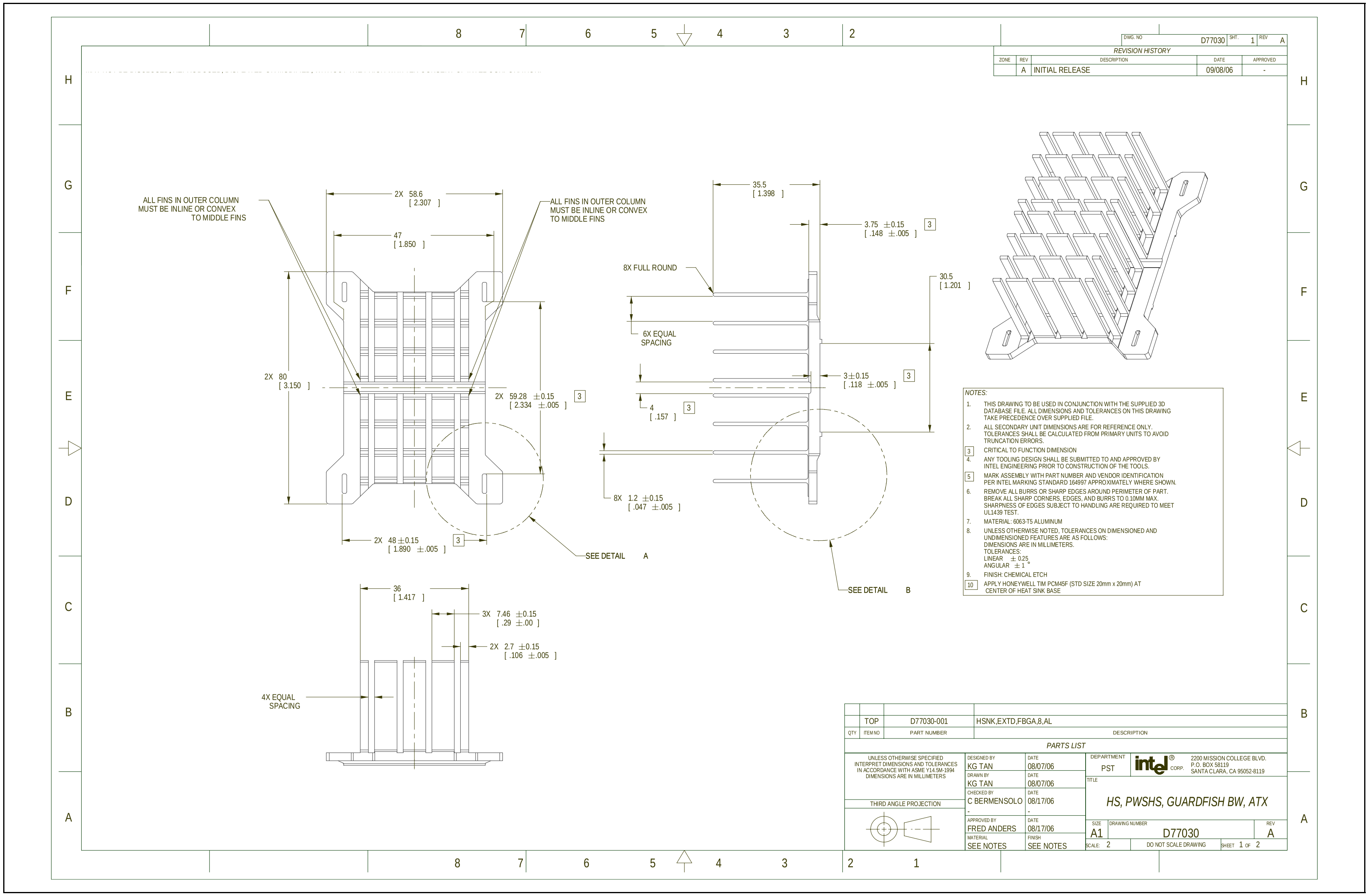


Figure 17. Intel® 3 Series Chipsets Reference Heatsink for ATX Platforms – Sheet 2

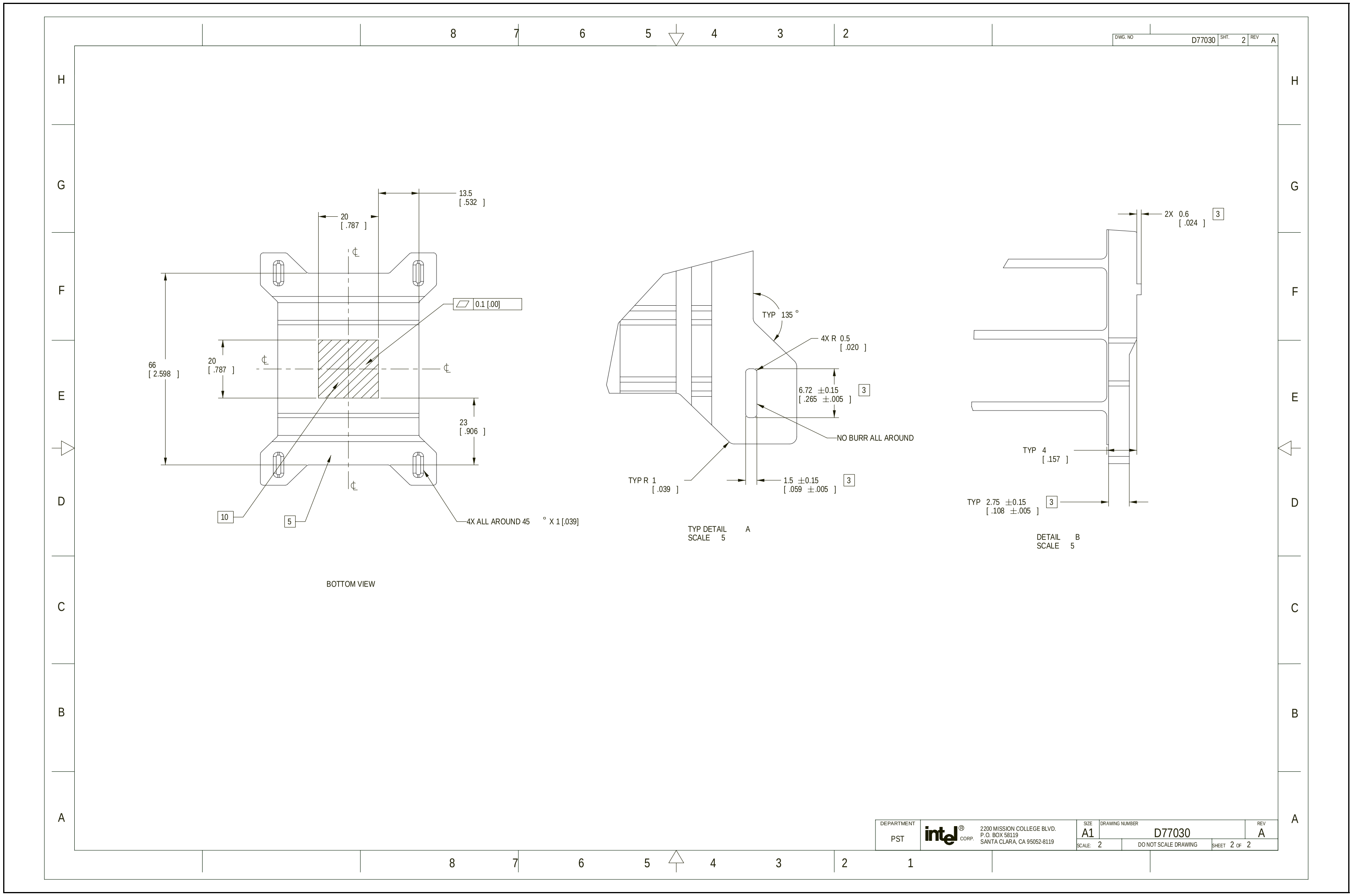
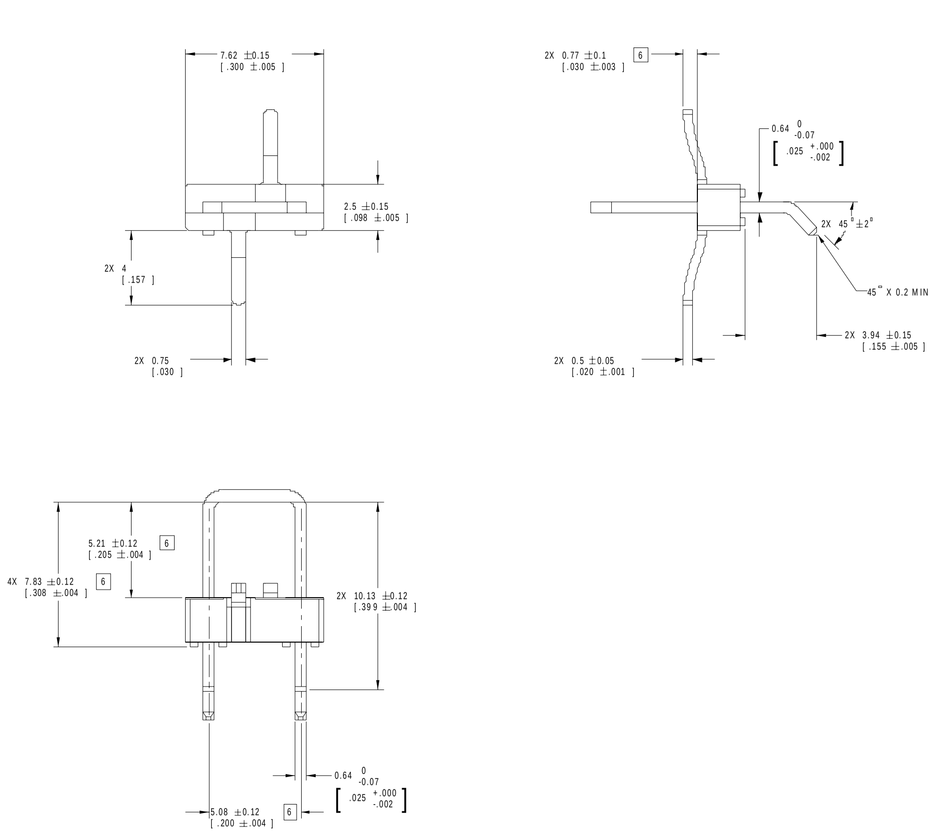
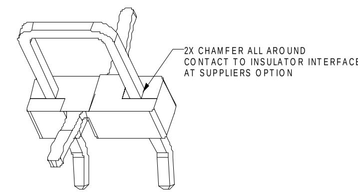


Figure 18. Intel® 3 Series Chipsets Reference Heatsink for ATX Platforms – Anchor





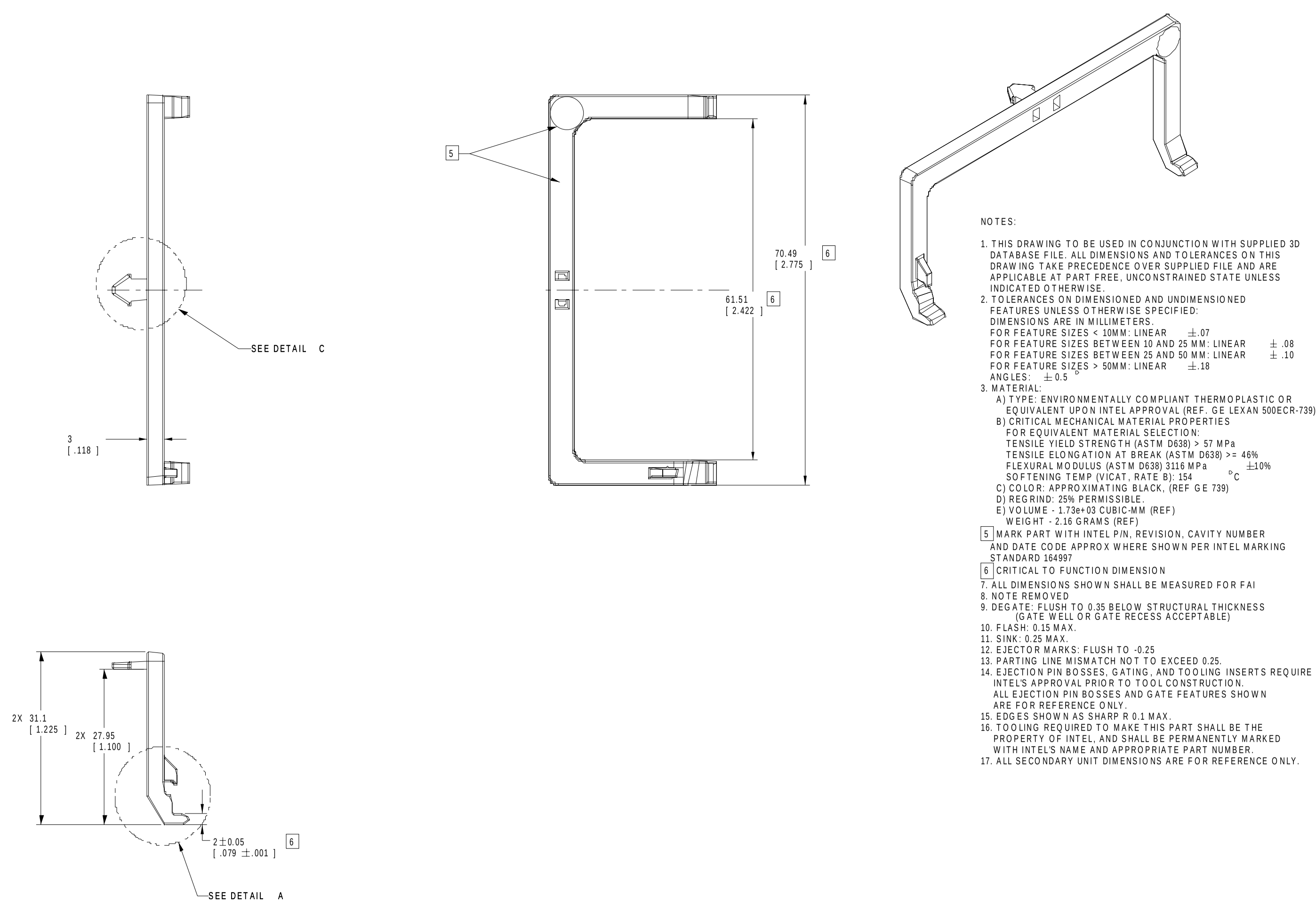
NOTES:

1. THIS DRAWING TO BE USED IN CONJUNCTION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE AND ARE APPLICABLE AT PART FREE, UNCONSTRAINED STATE UNLESS INDICATED OTHERWISE.
2. TOLERANCES ON DIMENSIONED AND UNDIMENSIONED FEATURES UNLESS OTHERWISE SPECIFIED:
   DIMENSIONS ARE IN MILLIMETERS.
   FOR FEATURE SIZES < 10MM: LINEAR ±.07
   FOR FEATURE SIZES > 10MM: LINEAR ±.08
   ANGLES: ± 0.5°
3. MATERIALS:
   INSULATOR: POLYCARBONATE THERMOPLASTIC, UL 94V-0, BLACK (739) (REF. GE LEXAN 3412R-739)
   CONTACT: BRASS OR EQUIVALENT UPON INTEL APPROVAL
   CONTACT FINISH: .000050u" MIN. NICKEL UNDER PLATING;
   SOLDER TAILS, 0.000100" MIN TIN ONLY SOLDER (LEAD FREE).
5. MARK WITH INTEL P/N AND REVISION PER INTEL MARKING STANDARD 164997; PER SEC 3.8 (POLYETHYLENE BAG)

$\boxed{6}$ CRITICAL TO FUNCTION DIMENSION

7. ALL DIMENSIONS SHOWN SHALL BE MEASURED FOR FAI
8. NOTE REMOVED
9. DEGATE: FLUSH TO 0.35 BELOW STRUCTURAL THICKNESS (GATE WELL OR GATE RECESS ACCEPTABLE)
10. FLASH: 0.15 MAX.
11. SINK: 0.25 MAX.
12. EJECTOR MARKS: FLUSH TO -0.25
13. PARTING LINE MISMATCH NOT TO EXCEED 0.25.
14. EJECTION PIN BOSSES, GATING, AND TOOLING INSERTS REQUIRE INTEL'S APPROVAL PRIOR TO TOOL CONSTRUCTION. ALL EJECTION PIN BOSSES AND GATE FEATURES SHOWN ARE FOR REFERENCE ONLY.
15. EDGES SHOWN AS SHARP R 0.1 MAX.
16. TOOLING REQUIRED TO MAKE THIS PART SHALL BE THE PROPERTY OF INTEL, AND SHALL BE PERMANENTLY MARKED WITH INTEL'S NAME AND APPROPRIATE PART NUMBER.
17. ALL SECONDARY UNIT DIMENSIONS ARE FOR REFERENCE ONLY.

Figure 19. Intel® 3 Series Chipsets Reference Heatsink for ATX Platforms – Ramp Retainer Sheet 1



NOTES:

1. THIS DRAWING TO BE USED IN CONJUNCTION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE AND ARE APPLICABLE AT PART FREE, UNCONSTRAINED STATE UNLESS INDICATED OTHERWISE.
2. TOLERANCES ON DIMENSIONED AND UNDIMENSIONED FEATURES UNLESS OTHERWISE SPECIFIED:
   DIMENSIONS ARE IN MILLIMETERS.
   FOR FEATURE SIZES < 10MM: LINEAR ±.07
   FOR FEATURE SIZES BETWEEN 10 AND 25 MM: LINEAR ±.08
   FOR FEATURE SIZES BETWEEN 25 AND 50 MM: LINEAR ±.10
   FOR FEATURE SIZES > 50MM: LINEAR ±.18
   ANGLES: ±0.5°
3. MATERIAL:
   A) TYPE: ENVIRONMENTALLY COMPLIANT THERMOPLASTIC OR EQUIVALENT UPON INTEL APPROVAL (REF. GE LEXAN 500ECR-739)
   B) CRITICAL MECHANICAL MATERIAL PROPERTIES FOR EQUIVALENT MATERIAL SELECTION:
      TENSILE YIELD STRENGTH (ASTM D638) > 57 MPa
      TENSILE ELONGATION AT BREAK (ASTM D638) >= 46%
      FLEXURAL MODULUS (ASTM D638) 3116 MPa ±10%
      SOFTENING TEMP (VICAT, RATE B): 154 °C
   C) COLOR: APPROXIMATING BLACK, (REF GE 739)
   D) REGRIND: 25% PERMISSIBLE.
   E) VOLUME - 1.73e+03 CUBIC-MM (REF)
      WEIGHT - 2.16 GRAMS (REF)

$\boxed{5}$ MARK PART WITH INTEL P/N, REVISION, CAVITY NUMBER AND DATE CODE APPROX WHERE SHOWN PER INTEL MARKING STANDARD 164997

$\boxed{6}$ CRITICAL TO FUNCTION DIMENSION

7. ALL DIMENSIONS SHOWN SHALL BE MEASURED FOR FAI
8. NOTE REMOVED
9. DEGATE: FLUSH TO 0.35 BELOW STRUCTURAL THICKNESS (GATE WELL OR GATE RECESS ACCEPTABLE)
10. FLASH: 0.15 MAX.
11. SINK: 0.25 MAX.
12. EJECTOR MARKS: FLUSH TO -0.25
13. PARTING LINE MISMATCH NOT TO EXCEED 0.25.
14. EJECTION PIN BOSSES, GATING, AND TOOLING INSERTS REQUIRE INTEL'S APPROVAL PRIOR TO TOOL CONSTRUCTION. ALL EJECTION PIN BOSSES AND GATE FEATURES SHOWN ARE FOR REFERENCE ONLY.
15. EDGES SHOWN AS SHARP R 0.1 MAX.
16. TOOLING REQUIRED TO MAKE THIS PART SHALL BE THE PROPERTY OF INTEL, AND SHALL BE PERMANENTLY MARKED WITH INTEL'S NAME AND APPROPRIATE PART NUMBER.
17. ALL SECONDARY UNIT DIMENSIONS ARE FOR REFERENCE ONLY.

Figure 20. Intel® 3 Series Chipsets Reference Heatsink for ATX Platforms – Ramp Retainer Sheet 2

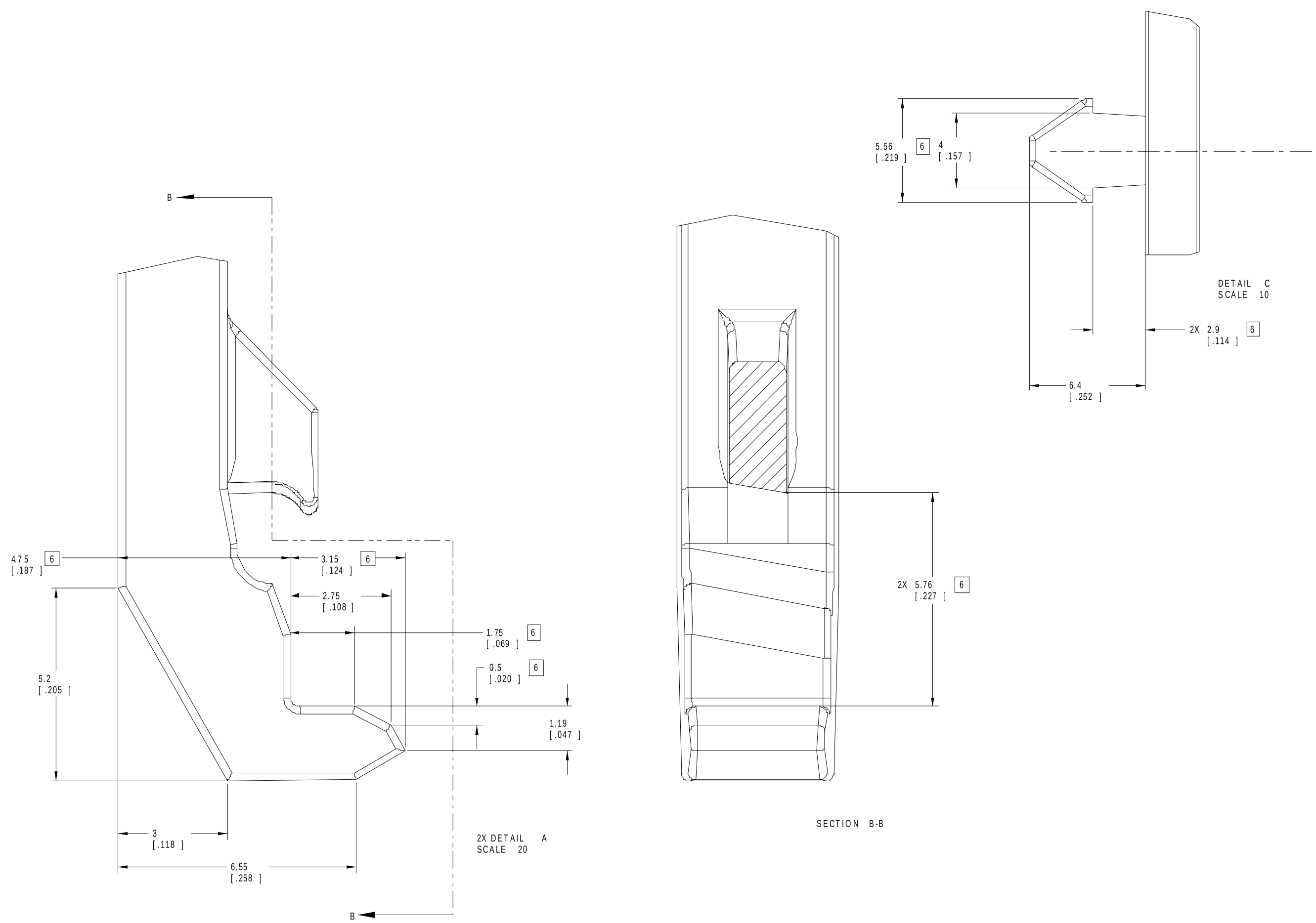


Figure 21. Intel® 3 Series Chipsets Reference Heatsink for ATX Platforms – Wire Preload Clip

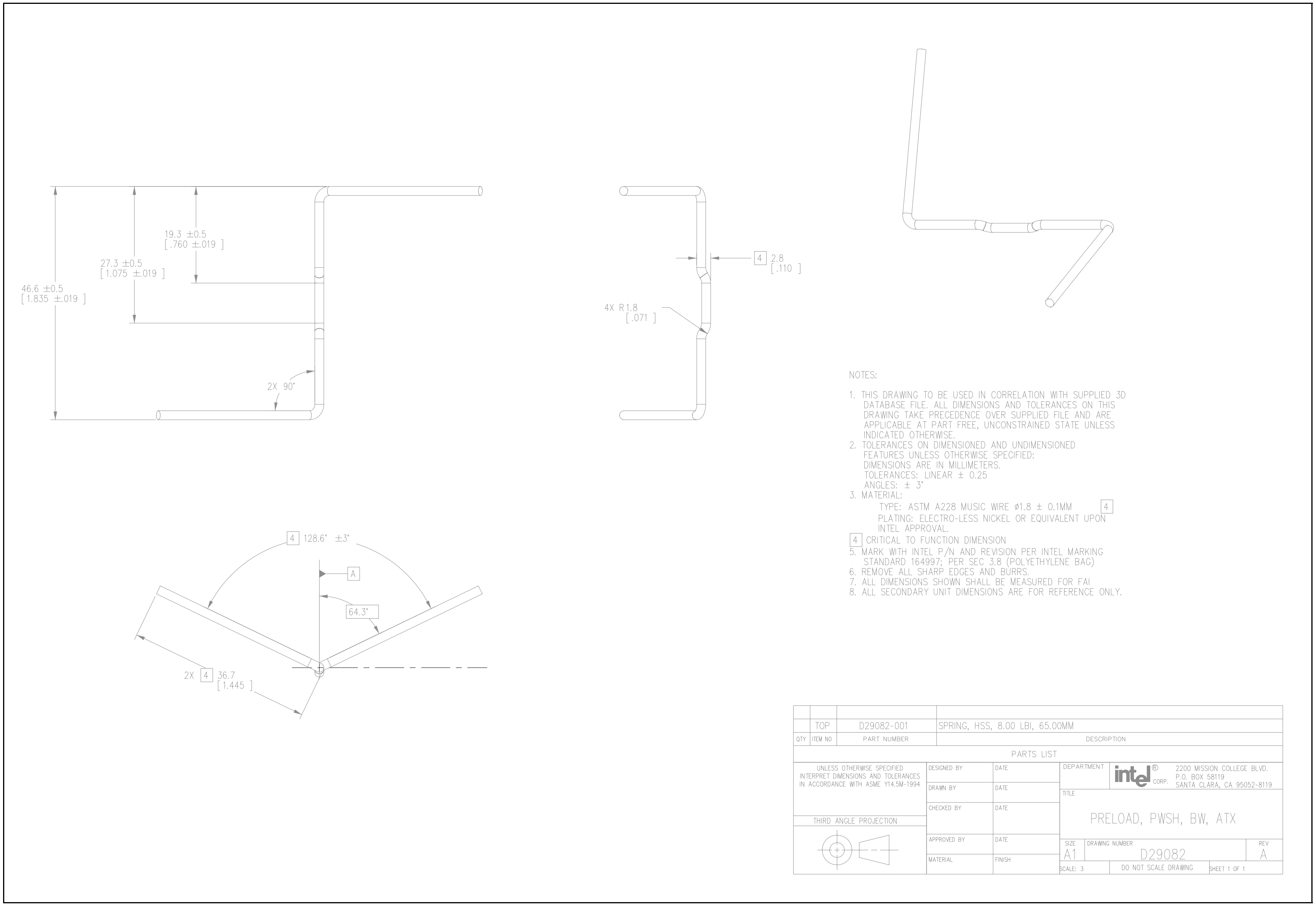


Figure 22. Intel® 3 Series Chipsets Reference Heatsink for Balanced Technology Extended (BTX) Platforms

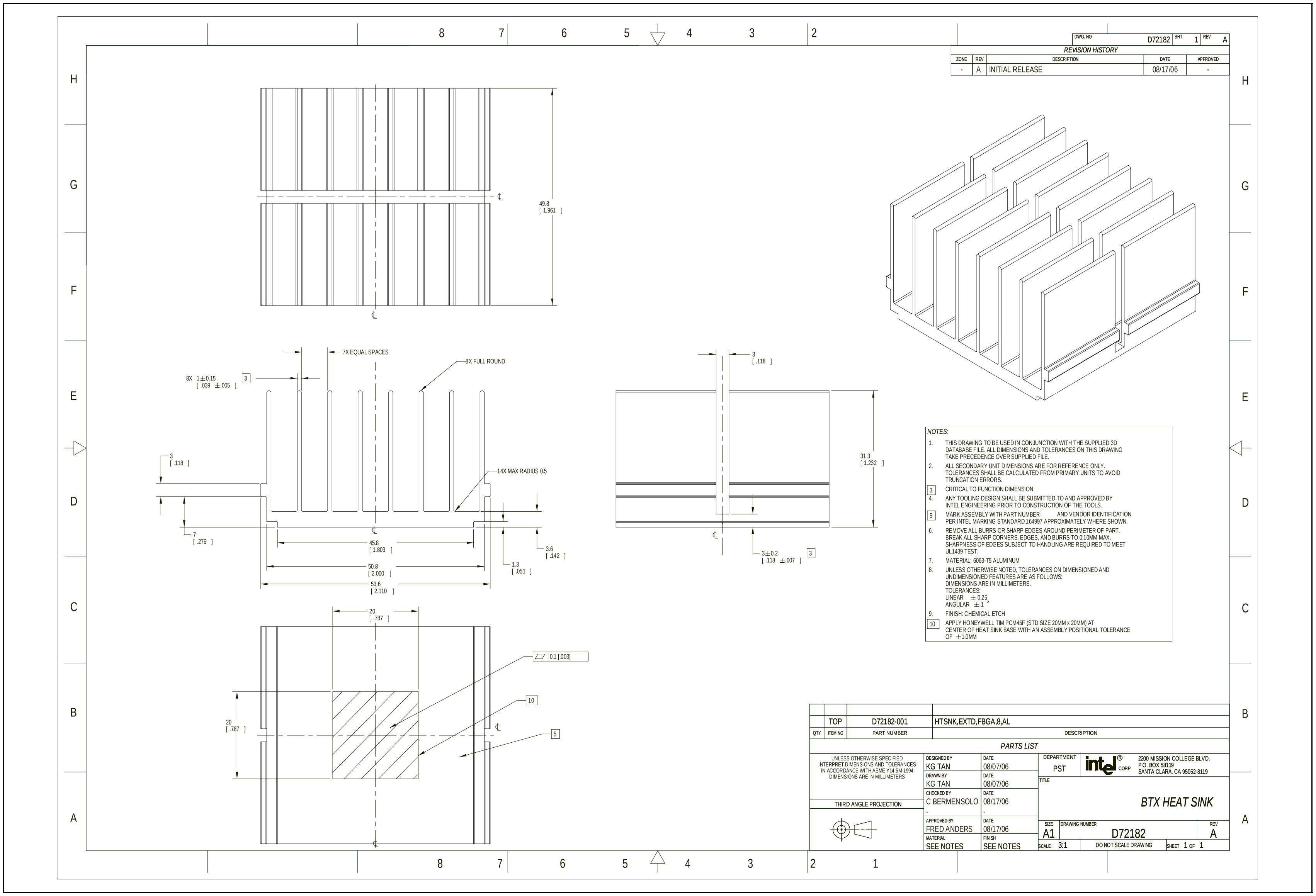
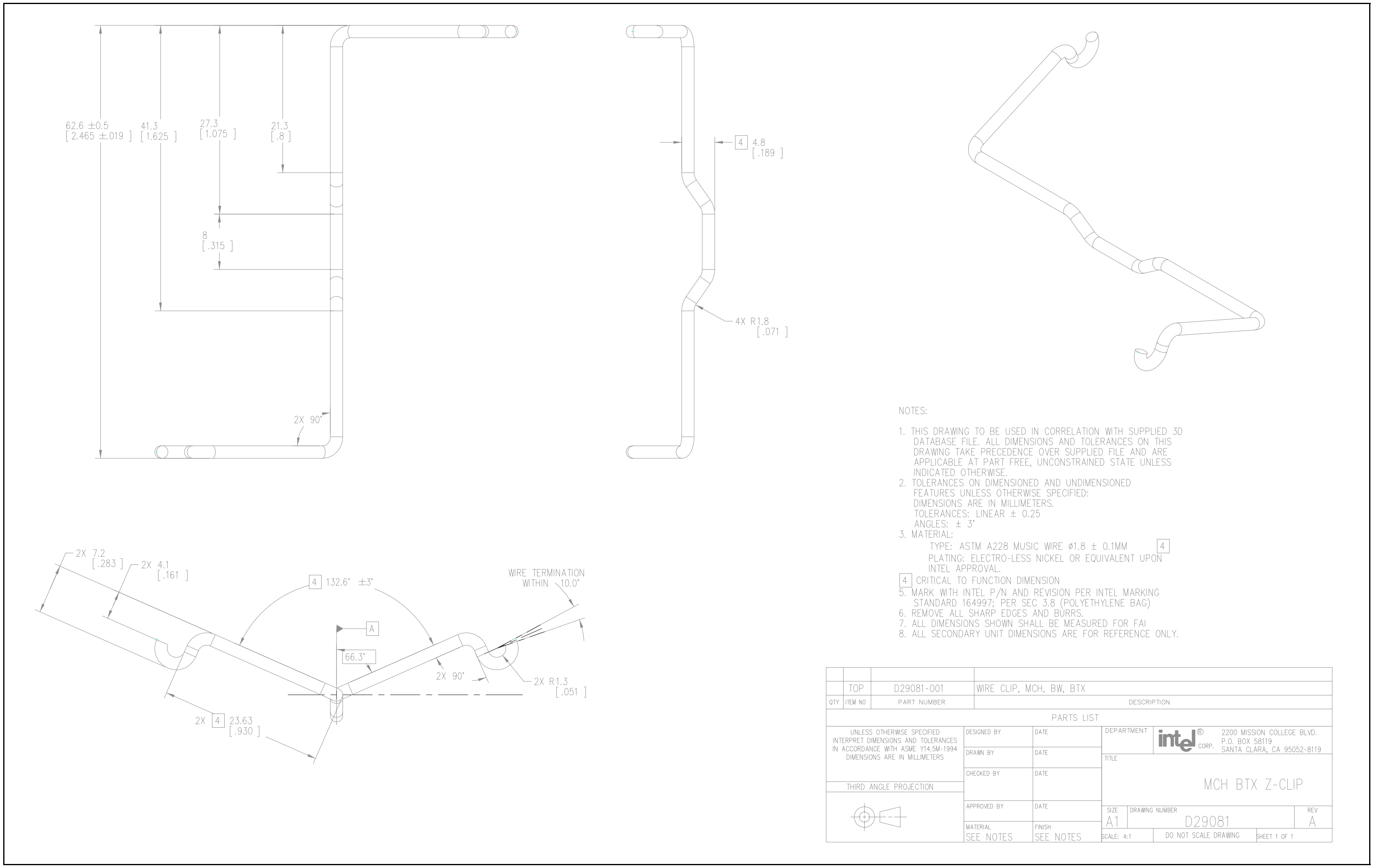


Figure 23. Intel® 3 Series Chipsets Reference Heatsink for Balanced Technology Extended (BTX) Platforms – Clip



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